PARALLEL PROCESSING: INTO THE NEXT

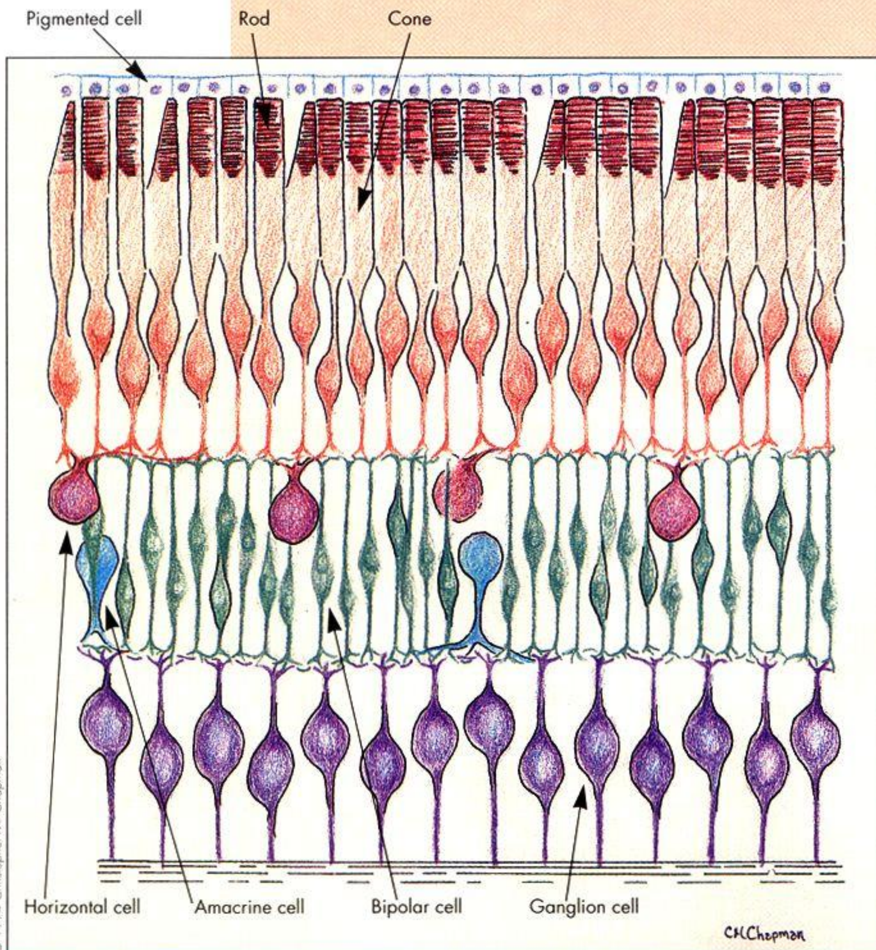

FIGURE 1. THE HUMAN RETINA.

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NATURAL SELECTION—IT IS NATURE'S RUTHLESS TOOL FOR OPTIMIZING SYSTEMS, YET ONE THAT ENCOURAGES DIVERSITY. AS ENGINEERS WE CAN STUDY THE STRUCTURE OF NATURAL SYSTEMS FOR CLUES THAT MAY LEAD TO THE OPTIMIZATION OF MAN-MADE SYSTEMS. ONE OF THE MOST INTRIGUING NATURAL OBJECTS TO STUDY IS THE HUMAN BRAIN AND ITS ASSOCIATED DISTRIBUTED PROCESSING SYSTEMS, SUCH AS THE EYES. IN A WORLD THAT EXISTS IN THREE DIMENSIONS, IT ISN'T AT ALL SURPRISING THAT THESE BIOPROCESSORS ARE HIGHLY PARALLEL, THREE-DIMENSIONAL (3-D) SYSTEMS.

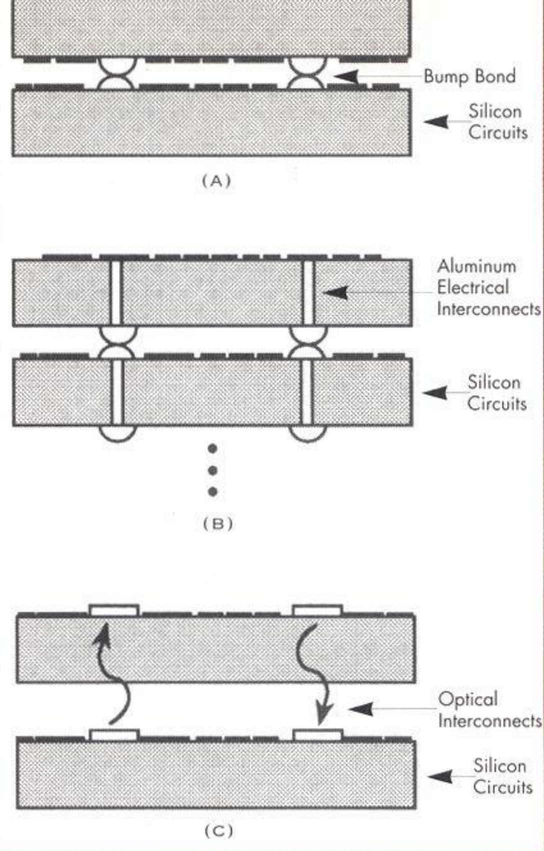


FIGURE 2. THREE-DIMENSIONAL INTEGRATION STRATEGIES: (A) FLIP CHIP USING BUMP BONDS; (B) ALUMINUM THROUGH-WAFER ELECTRICAL INTERCONNECT; (C) THROUGH-WAFER OPTICAL INTERCONNECT.

DIMENSION

BY NAN MARIE JOKERST

Although our engineered silicon processors are still largely two dimensional, the human brain provides a model of a three-dimensionally interconnected processor sheet approximately one meter square and five layers deep. Likewise, our retina (shown in Fig. 1) consists of one sensing (rods and cones), two processing (bipolar and ganglion), and two interconnection (horizontal and amacrine) layers that constitute a massively parallel, three-dimensionally interconnected imaging system.

Our challenge today is to identify the architectures, hardware, and algorithms that will set the stage for the next generation of engineered, massively parallel, three-dimensionally interconnected computational systems. A viable question is whether optics will play a lasting role in such commercial computational systems. Key to significantly shortening the path to useful systems is to encourage interaction at this early stage of development between all of the areas that influence one another so strongly in computational systems: Architecture, hardware, and software engineers. The probability that optics will play a role in these systems is significantly enhanced if we are involved at this point in the development of three-dimensional systems. We should work in parallel, but build a wealth of interconnections between ourselves and our colleagues!

Thin film devices offer a new way to integrate electrical and optical processing systems. This article explores how 3-D systems are currently connected and discusses how a new technique for creating, transferring, and bonding semiconductor devices to host substrates opens up a variety of architecture options for parallel processing.

THREE-DIMENSIONAL HARDWARE STRATEGIES

There are two basic approaches to connect multiple layers of electronic processing elements: electrical and optical. These interconnections can lie in the plane of the circuitry or perpendicular to it. Two-dimensional metallized interconnections are used in commercial semiconductor circuits. Waveguides can implement in-plane optical interconnections. To break into the third dimension, we will explore vertical electrical and vertical optical interconnections for electronic circuits.

The vertical electrical interconnection of multiple layers of low cost, high performance, very large scale (VLSI) circuits is emerging for two layers, and has been demonstrated in only one case for more than two layers. Standard VLSI circuits consist of a single crystal silicon substrate that contains the circuits, various layers of dielectrics and metals (there are usually at least two metal layers in today's VLSI), and polysilicon layers. Efficient circuit designs quickly cover the entire surface area of the silicon substrate with these materials; they cannot be used for nucleation for a second layer of silicon. Polysilicon on top of silicon circuits can serve as a sensor material,[1] but cannot host VLSI. This is one reason why laser recrystallization of polysilicon into single crystal silicon has been a significant research topic. Unfortunately, warm polysilicon and heat-damaged circuitry have been the primary results.

The need for growth nucleation sites can be avoided if two chips are physically stacked with the substrates attached. Flip chip bonding, illustrated in Figure 2(a), is one example of this approach. One chip is "flipped" and metal bumps bond the two chips together. Flip chip bonding has been used effectively by the military to "rule the night" with infrared focal plane arrays. In fact, these flip chip bonded focal plane arrays are some of the most advanced two layer systems that exist today, with 256 × 256 pixel detector arrays bump bonded to VLSI circuits to make them smart (hence the name "smart pixels").[2] The metal bumps electrically interconnect the inwardly facing circuitry and detectors—the substrates of the two layers facing out-

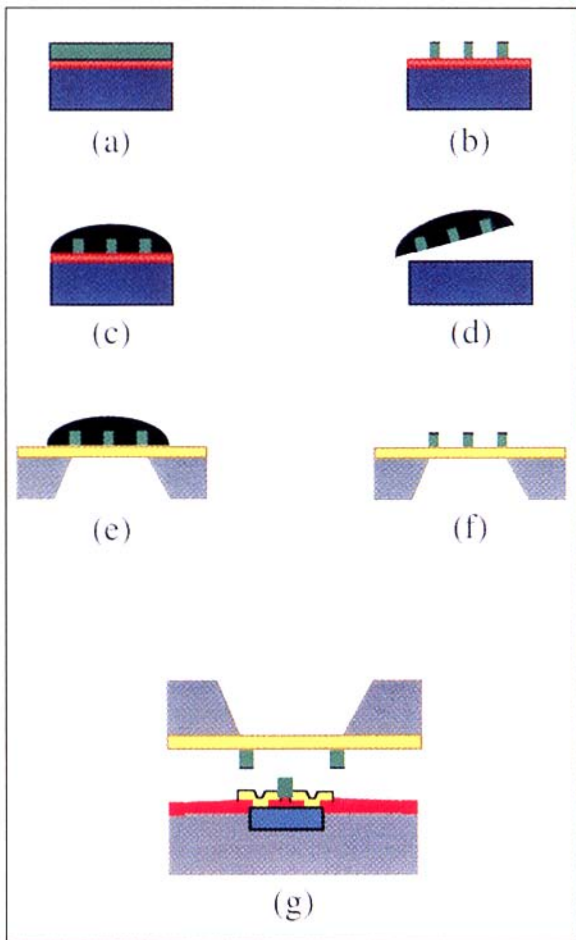


FIGURE 3. ILLUSTRATION OF THIN FILM SEPARATION AND TRANSFER DIAPHRAGM PROCESS: (A) AS-GROWN SAMPLE WITH EPILAYERS OF INTEREST ON TOP AND SACRIFICIAL ETCH LAYER BETWEEN EPILAYERS OF INTEREST AND GROWTH SUBSTRATE; (B) MESA-ETCHED EPILAYERS; (C) SAMPLE COATED WITH BLACK WAX; (D) SACRIFICIAL LAYER IS ETCHED, THUS SEPARATING EPILAYERS FROM GROWTH SUBSTRATE; (E) EPILAYERS ARE BONDED TO TRANSPARENT TRANSFER DIAPHRAGM; (F) BLACK WAX IS REMOVED FROM THIN FILM DEVICES ON DIAPHRAGM; (G) THIN FILM DEVICES ARE ALIGNED AND BONDED TO HOST SUBSTRATE.

ward. These systems are, however, limited to two layers since the outward facing substrate sides are not individually connected to the inside of the stack.

A strong advantage and weakness of flip chip bonded systems is that any two materials can be bump bonded to one another without any nucleation or lattice matching constraints. For focal plane arrays, mercury cadmium telluride (HgCdTe), which operates in the mid-infrared, is often used for the focal plane detector array, and silicon or gallium arsenide (GaAs) is used for the circuits. This is an example of how the cost and performance of a system can be significantly improved if the engineer is given the freedom to use the optimal material for the job. In the focal plane array case, silicon doesn't detect in the mid-infrared, and HgCdTe VLSI circuitry doesn't exist! The weakness with the bump bonding of different materials lies in the difference between the coefficient of thermal expansion of the two materials. When two bump bonded substrates composed of different materials are heated or cooled, the expansion or contraction of the two materials may differ enough to cause failure of the bump bonds. This bump bond failure is a limiting factor on the size of any single focal plane array. Bump bonding numerous smaller arrays of detectors to circuitry (called tiling) may be an effective solution to this problem.

The real goal of three-dimensional integration, however, is to connect more than two processing layers. As indicated by our brain and eye structures, we don't need to form computer cubes; three to five layers of processing are enough for many purposes. Three-dimensional vertical electrically connected computational hardware with five layers of processing, two of which are illustrated in Figure 2(b), has been recently demonstrated.[3] The key to this hardware is to provide isolated electrical connections from the back to the front of the silicon wafers that are then stacked. Before integrating circuitry onto the silicon, these vertical electrical channels are formed using droplets of aluminum that are thermally encouraged to flow from one face of the silicon wafer to the other. These channels become p-type, which, in n-type silicon, electrically isolate the channels from each other. This also gives the channels fairly high capacitance. The circuitry is then integrated onto one side of the silicon substrate, an electrically conducting spring is attached to

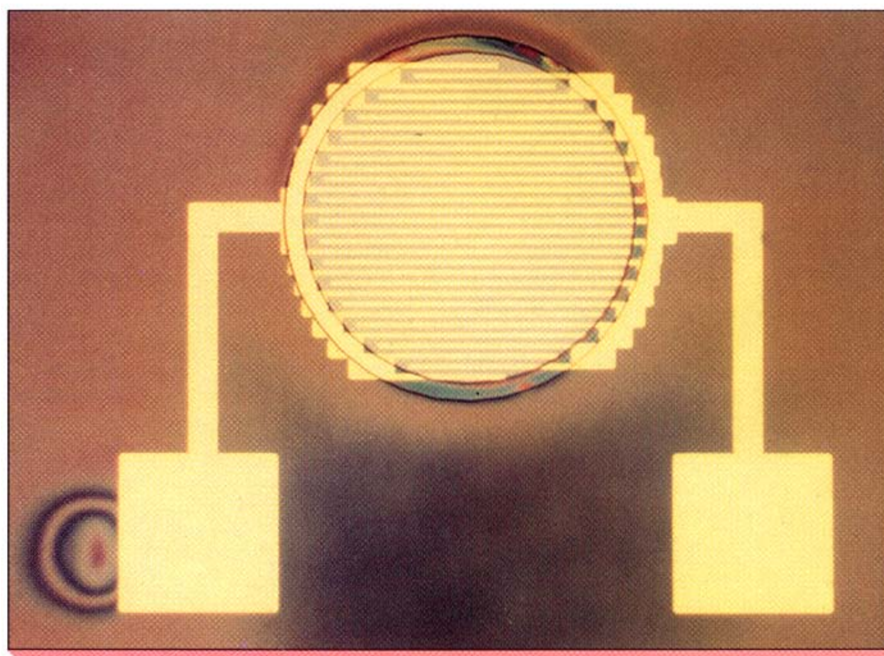


FIGURE 4. THIN FILM INGAASP METAL-SEMICONDUCTOR-METAL DETECTOR INTEGRATED ONTO SILICON HOST SUBSTRATE.

the electrical feedthroughs on the back of the substrates, and the substrates are mechanically stacked to form the 3-D system.

Vertical interconnections between layers of circuitry can also be accomplished using optical signals. Optical interconnects can have many advantages, including high bandwidth, low crosstalk, low capacitance, and electrical isolation. Two basic types of vertical optical interconnects have been demonstrated between two physically separate circuits: reflective and transmissive. In either case, emitters, modulators, and/or detectors must be integrated with the silicon circuitry to move toward the goal of a self-contained system in which only electrical power is supplied. The reflective cases can use the optical signal from one silicon processing surface to connect to another surface through reflection or holography. Reflection-based schemes include interconnection external or internal (using total internal reflection) to the substrate. Transmissive interconnects, by contrast, are limited to wavelengths of low optical loss. One interesting type of transmissive interconnect uses optical wavelengths that are not absorbed by silicon. This interconnect channels the optical beam directly through the wafer, as shown in Figure 2(c). This was first demonstrated using external lasers[4] that operate at wavelengths longer than about 1.1 µm, which corresponds to energies smaller than the bandgap energy of silicon (so the light is not absorbed). Completely integrating the light source into these systems is difficult due to the lattice constants involved: the compounds that emit at the wavelengths needed are not lattice matched to silicon. It is possible to fabricate a detector of these materials using direct growth, but the growth of efficient emitters at these wavelengths onto silicon—a must for minimizing waste heat—has not yet been demonstrated.

An alternative transmission scheme uses grating-coupled waveguides that lie above or below the silicon circuitry. These waveguide optical interconnect layers can serve as routing and signal processing layers between layers of silicon circuitry, with the gratings coupling the optical signal vertically to and from the silicon circuits. But once again, for self-contained systems, efficient optical emitters, detectors, and modulators integrated onto the silicon circuit are essential for 3-D hardware.

In this quest for integrating optoelectronic components with silicon, or mixed materials systems, a new technique for creating, transferring, and bonding thin film semiconductor devices to host substrates (such as silicon circuits) has recently emerged. These thin film devices are fabricated using a technique named epitaxial lift off (ELO). In this process, high-quality, often lattice-matched, materials are separated from the growth substrate using selective etching. These thin film devices can then be bonded to arbitrary host substrates without any need for lattice matching. The goal of this integration technology is to produce inexpensive, high performance mixed material integrated systems, which include massively parallel three-dimensional systems. To achieve high performance, single crystal material that is not degraded by the fabrication process is used. For low cost, manufacturable integration, standard materials and processes are used and process steps minimized.

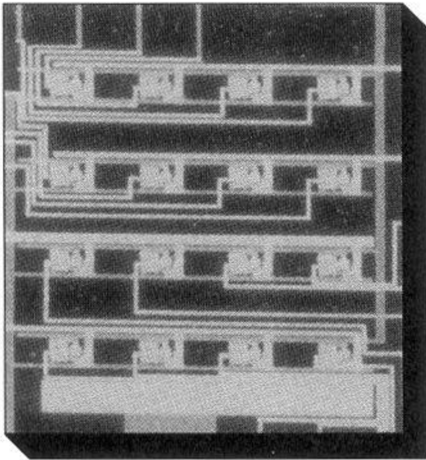
Thin Film Device Fabrication, Transfer, and Bonding

Many optical and electrical devices are fabricated from epilayers (layers of material, usually single crystal, grown on a substrate) that do not need the growth substrate for optimal operation. The ELO process is used to separate these single crystal epilayers from the growth substrate using a sacrificial or stop etch layer combined with selective etches.[5] Using handling layers and transfer techniques, these epilayers, which are thin film materials on the order of microns thick, can be handled with tweezers after separation, processed on both sides of the device, aligned, and bonded onto arbitrary host substrates.

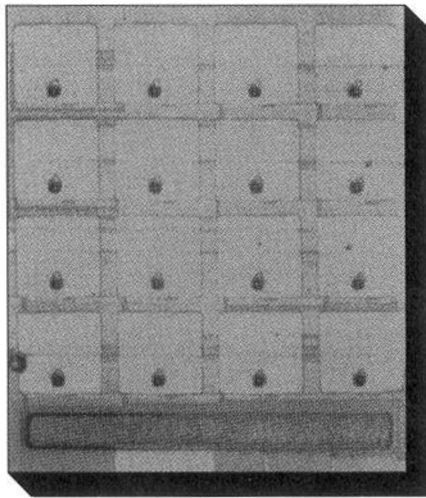
The ELO process is illustrated in Figure 3. The "as-grown" material, with the epilayers of interest on top of the sacrificial etch layer, is shown in Figure 3(a). The first step in the ELO process is to apply any top contacts or coatings desired on the as-grown material and define the individual devices through mesa etching, as shown in Figure 3(b). The next step is to coat the sample with a black wax handling layer, as seen in Figure 3(c), by either melting or spray coating the wax onto the material. The sample is then immersed into the selective etch solution, which etches away the sacrificial layer, thus separating the epitaxial layers from the growth substrate (illustrated in Figure 3(d)). High quality thin films as large as 2 cm × 4 cm[6] and films as thin as 200 Å[6] to as thick as 4.5 µm[7] have been reported. After the epitaxial thin film has been separated from the growth substrate, it is bonded to a host substrate. Once bonded, the black wax coating is removed.

A modified ELO technique using a transfer diaphragm[8] is shown in the remainder of Figure 3. Using this technique, both sides of the thin film material can be processed while under substrate support. In addition, single devices can be aligned and selectively deposited from an array of devices or the entire array can be simultaneously aligned and deposited. The mesa etch, coating and separation steps in the ELO process remain unchanged. The next step, however, is different: the array of thin film devices, embedded in the black wax, is contact bonded to a transparent transfer diaphragm, shown in Figure 3(e), and the black wax is removed to reveal the thin film devices, as in Figure 3(f). To transfer and bond these thin film devices to the host substrate, the transparent diaphragm is inverted so that the devices face the host substrate. The thin film devices are visually aligned and a pressure probe is applied to the diaphragm to transfer an individual device from the array, a subarray, or the entire array of devices to the host substrate, as illustrated in Figure 3(g).

This process inverts the devices, so that the side of the device that was processed before separation is now bonded to the host substrate. This is particularly useful for the bonding process since a metal contact on the host substrate and a metallized thin film device will form a stable electrical and mechanical bond that, in preliminary tests, has also shown high thermal conductivity. In fact, this can be regarded as a thin film device with a very thin bump bond. After bonding, the exposed side of the thin film device can be processed using standard



5(A)

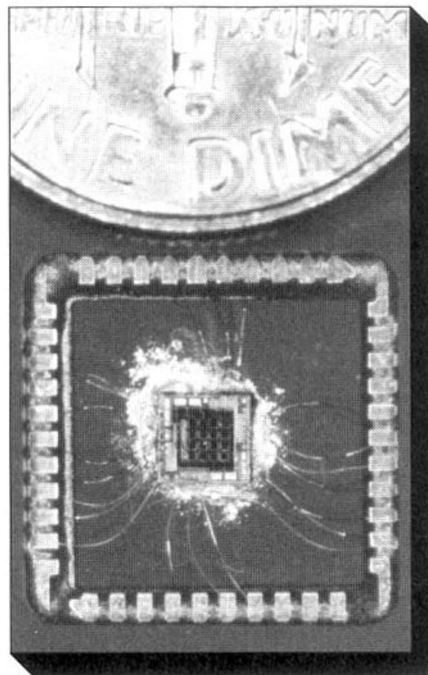


5(B)

FIGURE 5. THREE-DIMENSIONAL, VERTICALLY ELECTRICALLY INTERCONNECTED NEURAL NETWORK IMAGING ARRAY: (A) SILICON NEURAL OSCILLATOR CIRCUIT; (B) SILICON CIRCUIT PLANARIZED WITH POLYIMIDE, VIAS ETCHED INTO POLYIMIDE, AND METALLIZED; (C) THIN FILM DETECTORS WITH TOP CONTACT BONDED ONTO THE METALLIZED PADS ON THE POLYIMIDE. NOTE THAT EACH DETECTOR IS CONNECTED TO THE SILICON OSCILLATOR CIRCUIT THAT LIES DIRECTLY UNDERNEATH IT.

microfabrication techniques to form electrical contacts and/or optical coatings. For example, Figure 4 is a photomicrograph of an InGaAsP metal-semiconductor-metal detector that is bonded to a silicon substrate coated with insulating silicon dioxide. This detector, 100 µm in diameter (about the same as a human hair) and 1 µm thick, senses 1.3 µm wavelength light to a modulation frequency of 950 MHz.[9]

A useful analogy for the transfer diaphragm technique is that of the "rub-on" letters that were used to insert nonstandard symbols into standard text (before the advent of typeset changeable typewriters and word processors). The standard text was written using an inexpensive typewriter, which parallels the low cost mass production of complex silicon integrated circuitry in foundries today. The less often used mathematical symbols (represented by compound semiconductor devices) were applied selectively from a sheet of rub-on letters because standard typewriters lacked enough space for Greek symbols. Using this technique, a host of different symbols could be placed on a single page of text by aligning and transferring the desired symbols onto the page. In the same manner, multiple material and multiple function thin film devices can be integrated onto a single host substrate, such as a silicon circuit, using the transfer diaphragm technique. A single epitaxial growth of thin film devices can be fabricated into an array of devices, and a large number of host substrates can be integrated through selectively bonding a single device from the array of devices. Thus, the cost of the epitaxial growth can be distributed across a large number of integrated systems just as one large sheet of rub-on "λs" were enough for an entire optics text!



5(C)

Thin film device integration has excellent potential for low cost, high performance integrated optoelectronic systems. High yield can be achieved through pretest of the thin film devices and the host substrate before integration, and the thin film devices bonded to a host substrate can be repaired if they are faulty.[9] Wafer scale integration can be achieved by aligning and bonding highly uniform, smaller subarrays of thin film devices. This eases the need for wafer scale growth uniformity for wafer scale integration. For high performance, a number of investigations have examined the quality of these thin film materials and devices after separation and processing,[10-15] and the material quality remains high. There are no lattice constant constraints on the host substrate, which can be, for example, an amorphous glass or a polymer. There are significant performance advantages in multimaterial systems since the individual materials and components can be independently optimized. To date, thin film AlGaAs, InGaAsP, CdTe, CdS, and Si-based materials and devices have been bonded to host substrates that include silicon, lithium niobate, glass, and polymers. These compound semiconductor devices include detectors, light emitting diodes, lasers, modulators, passive optical components, and circuits. Enhanced performance can often also be achieved by removing the substrate. Metal-semiconductor-metal detectors can be fabricated with the contact fingers on the bottom of the device, where they no longer shadow the incident signal.[16] Lasers, light emitting diodes, detectors, and modulators can all achieve high performance through use of a resonant cavity. Since both sides of thin film devices can be

coated, inexpensive, manufacturing-tolerant vacuum-deposited multilayer coatings can be used for optimal anti- or high-reflectivity mirrors.[17]

THREE-DIMENSIONAL INTERCONNECTS USING THIN FILM DEVICES
ELO devices offer a unique opportunity for three-dimensional vertical electrical and vertical optical interconnections. For vertical electrical interconnects, these thin film devices can be integrated directly on top of silicon circuitry with a layer of planarizing insulating material that lies between the thin film devices and the silicon circuitry. One example of a signal processing system that will benefit from this three-dimensional connection is optical imaging arrays. These arrays can take advantage of the parallel connection of each detector to signal processing circuitry, thus increasing throughput and processing speed through parallel processing. The vertical optical interconnection of layers of silicon uses thin film emitters and detectors that operate at a wavelength (1.3 µm) to which the silicon is transparent.

A schematic and photomicrographs of a thin film, three-dimensional, vertically electrically interconnected circuit are shown in Figure 5. The silicon circuit, fabricated at a silicon circuit foundry, is a retina-based neural network chip. The output of each oscillator circuit in the array is proportional to the current input level from the detector integrated directly on top of that oscillator. To fabricate the three-dimensional integrated circuit, the silicon circuit shown in Figure 5(a) was spin coated with planarizing insulating polyimide.[18] Using standard photolithography and plasma etching, vias (holes) were defined in the polyimide that exposed the underlying aluminum pads on the circuit. Metals were then vacuum deposited to electrically connect the underlying circuit to the top of the polyimide, as shown in Figure 5(b). This figure shows the contact pads for the thin film device on top of the polyimide. Note the dark spot in each of the pads—the metallized vias that will connect each oscillator in the silicon circuit to the detector that lies directly above it. The transfer diaphragm technique was then used to align and bond the thin film AlGaAs/GaAs/AlGaAs p-i-n detector array to the pads on the polyimide. To complete the integration, the common top metal contact was deposited and windows in this contact opened. Using this fabrication technique, each detector pixel in the array is vertically electrically connected to the circuitry that lies directly below. Every pixel in this smart pixel array, shown in Figure 5(c), was functional, with outputs over seven decades. The same techniques were used to create the 3-D interconnected 8 x 8 array shown on the cover.

Vertical optical interconnections through stacked silicon wafers have also been demonstrated using thin film device bonding to silicon. This through-silicon wafer interconnection has been demonstrated with thin film InGaAsP/InP-based emitters and detectors operating at a wavelength of 1.3 µm integrated onto silicon host substrates.[7] The devices were separated from the growth substrate, inverted, and bonded to two separate 650 µm-thick, polished, nitride coated, metallized silicon host substrates. Windows in the detector, emitter, and host wafer metallizations were aligned, and the two silicon wafers were stacked with the detector bonded wafer on top. The thin film emitter bonded to the bottom silicon wafer emits through the silicon wafer that lies above it. The light passes unabsorbed through this silicon substrate and is sensed by the detector, which is bonded to the top silicon substrate. Although the system power conversion efficiency of 4×10^{-7} was low for this first unoptimized demonstration, improvements in the optical system will improve this efficiency considerably.[7] Efficient optical interconnect is key to relieving the thermal load in this system, which is a major engineering issue.

CONCLUSION
Natural computational systems evolved with three-dimensional interconnections readily accessible, and have taken advantage of these inter-

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connections as evidenced by the brain and retina. Man-made computational hardware is currently restricted to two dimensions, but the limitations of these systems are apparent, and the drive toward massively parallel, three-dimensionally interconnected systems has been initiated. The addition of optical interconnections to existing hardware offers a simple method for introducing the third dimension to systems, but, since silicon dominates computational hardware, mixed material systems offer the simplest path to fully integrated optical interconnection. These mixed material systems can be achieved through bonding thin film devices to host substrates such as circuitry, thus realizing three-dimensional interconnections. Beyond solving the dilemmas that face computation today, this evolution into the next dimension may be the critical step toward brain-like computational abilities that will set this new generation of computers apart from its ancestors.

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