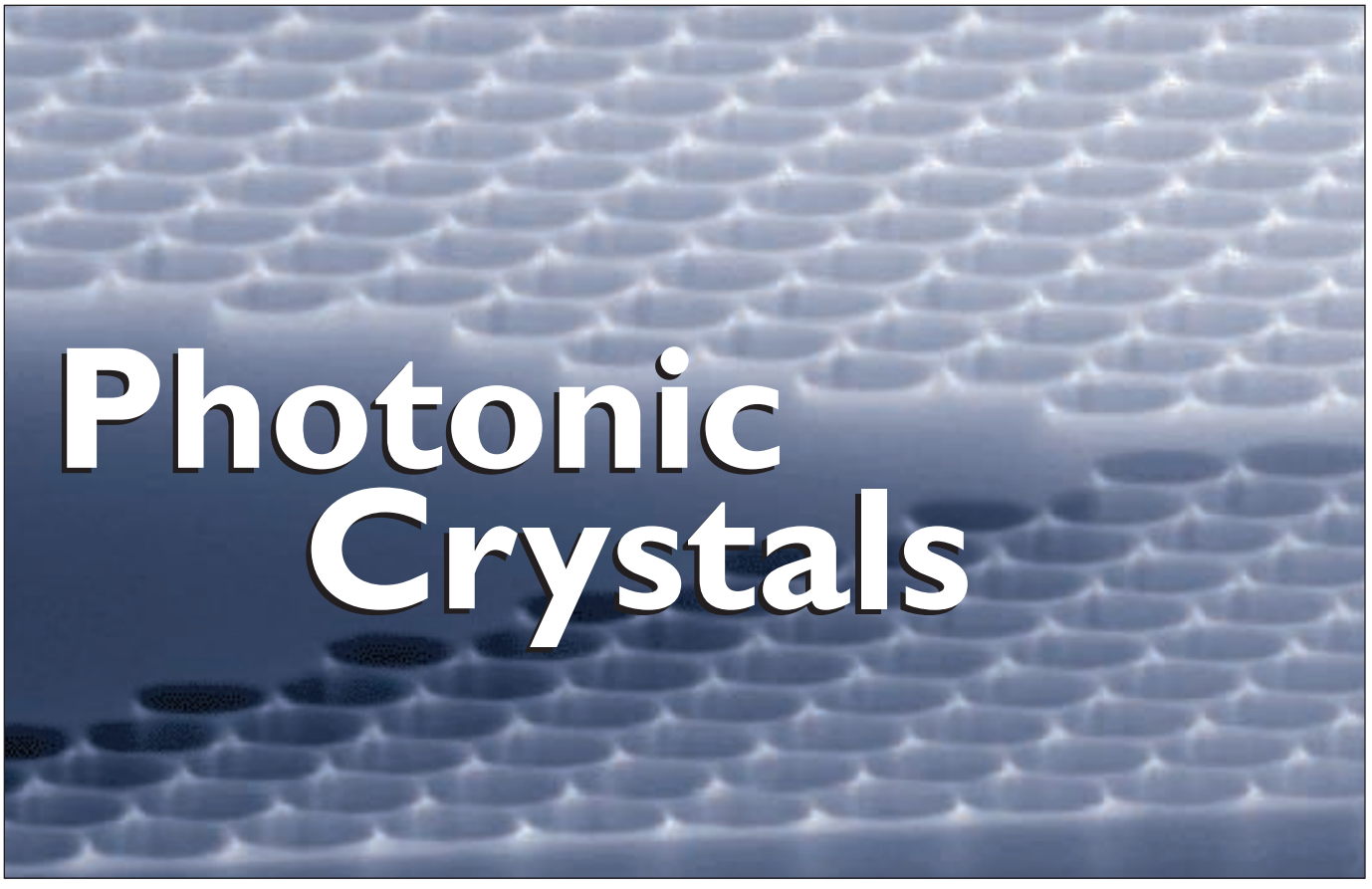

# Photonic Crystals

## *An Engineering Perspective*

**Dennis W. Prather**

**Photonic crystal devices possess a unique ability to control and localize light. This article discusses design and fabrication methods used to engineer photonic crystal devices for use in chip-scale photonic systems.**

In recent years, the dominant force in driving technical innovation has been the telecommunications industry. While some aspects of this industry drive technologies that span the globe, others drive technologies smaller than the eye can see. Although collectively, these technologies have revolutionized the field of telecommunications, further advances in device technology are needed before the goals of next-generation systems can be achieved. To address this need, new technology areas such as micro-fluidics, MEMS, and micro- and nano-optics have emerged. While each of these technologies has unique advantages, few hold the promise of photonic crystal (PhC)—or photonic bandgap (PBG)—devices, which possess a unique ability to localize and control light. This ability is coupled with the fact that PhC devices in the near-infrared regime are inherently very small, with critical dimensions typically on the order of 300-400 nm. For this reason, PhCs offer the ability to control light effectively, while at the same time being suitable for direct, chip-scale integration. They also have a unique ability to incorporate wavelength-dependent functionality over a very small operational volume. These important characteristics explain why PhCs are generating interest in the context of next-generation optoelectronic systems.

One driving application is the chip-scale photonic network, which aims primarily to emulate macroscopic devices and technologies. The motivation behind this approach is that optical-fiber networks, by virtue of their ability to offer a communication infrastructure with significantly higher bandwidth at significantly lower loss, have had a profound impact on the field of telecommunications. The same need is arising on the chip-scale level as chip speeds rise into the tens of GHz regime, as recently demonstrated by IBM's SiGe technology. In addition to increased clock speed, thanks to the advent of extreme ultraviolet lithography, the density of next-generation integrated circuits is likely to be nearly an order of magnitude larger. As a result of these two enabling trends, by incorporating more sophisticated aspects of instructional level parallelism and multiple processors in memory, next-generation computer chips will possess significantly more complicated architectures. These systems will therefore become highly interconnected, high-speed,


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chip-scale networks in need of a communication infrastructure similar to that used in optical-fiber networks.

Naturally, there is a notable difference between the scale of optical-fiber technology and that which is needed for chip-scale operations. To construct a chip-scale optical network, an optical infrastructure must be realized on a scale commensurate with the submicrometer dimensions of chip-scale components. Because of its unique ability to incorporate wavelength-dependent functionality over a very small operational volume, PhC technology offers significant promise in this arena. But before chip-scale photonic networks can become a reality, a number of technological barriers must be overcome. These include development of: repeatable and reliable design tools, high-fidelity fabrication processes, high-efficiency input- and output-coupling structures, and manufacturable integration processes. To varying degrees, each of these issues is being addressed by the research community. In the remainder of this article, I will review some of the more prominent developments in each area.

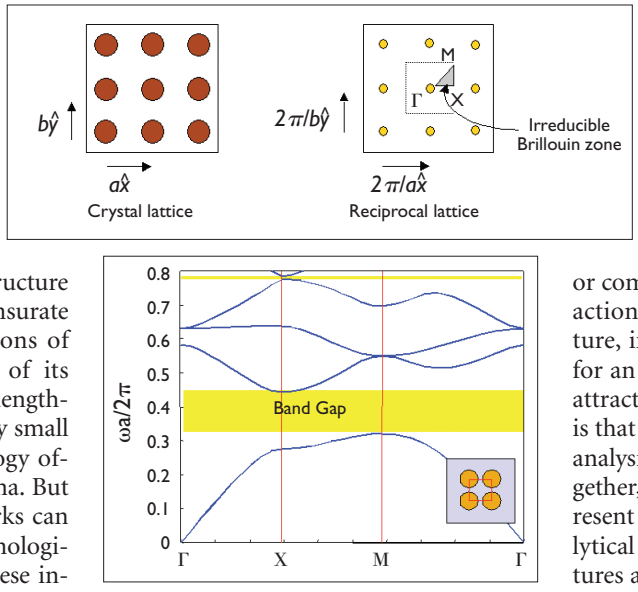


**Figure 1**. (a) Diagram of a 2D rectangular lattice and its representation in the reciprocal space, and (b) dispersion diagram of a rectangular lattice

## Design tools

The development of design and analysis tools for PhCs has a very interesting history. When Eli Yablonovitch first proposed the idea of photonic crystals,[1] tools for their design did not exist. As a result, the search for the first PhC structure was largely an experimental endeavor based on trial and error. The first theories of PhC analysis were developed largely by the solid-state physics and band-theory communities.[2] For this reason, many of the descriptive terms for PhCs are analogous to similar references in band theory: dispersion diagrams, Brillouin zones, and reciprocal lattices (see Fig. 1). In fact, early work in this regard focused on applying the same mathematical tools to PhC structures that had been used to calculate the band diagrams for semiconductor materials. But due to the vector nature of electromagnetic fields, these early tools proved inaccurate.

Mathematical tools that incorporated the vector nature of electromagnetic fields were later developed and showed good agreement with early experimental results. These tools were based in large part on a technique known as the plane wave method (PWM), in which an assumption of periodicity is made within the lattice. Because the PhC lattice is inherently periodic, this is a valid assumption. However, once a defect—such as a channel defect or an arbitrary irregularity (or point defect)—is added into the lattice, the assumption is no longer valid. Remarkably, the PWM is still very useful for some types of defects, namely, those that can be incorporated into a larger unit (or supercell). Maintaining the assumption of periodicity, if the supercell is large enough, i.e., if an adequate number of neighboring cells are incorporated into it, the fields localized within the supercell are electromagnetically isolated from their periodic neighbors. As a result, in some cases, good agreement is still found using the PWM. However, there is a significant computational cost involved in applying the PWM to supercell structures, particularly in three dimensions. For this reason, alternate tools were also developed and applied to PhC analysis. Many such tools are described in the literature; one of the more common is the finite-difference time-domain method (FDTD).[3]

The FDTD method is different from the PWM in that it makes no assumption of periodicity. Having said this, it is possible to incorporate periodic boundary conditions into the FDTD method if one determines that by doing so one accurately represents the physics of the problem. In essence, the FDTD method discretizes the differential forms of Faraday's and Ampere's laws, and maps them onto an interlaced grid (see Fig. 2). At this point, the incident field is time marched through the grid, or computational domain, until the interaction between the fields and the structure, in our case a PhC structure, allows for an accurate analysis. One of the more attractive attributes of the FDTD method is that it can incorporate a complete band analysis in a single computational run. Together, the PWM and FDTD methods represent a substantially complete set of analytical tools for the design of PhC structures and devices. Once designed, however, the devices must be fabricated. Fabrication techniques are discussed next.

## Fabrication methods

Early efforts to fabricate PhC structures focused on drilling arrays of tilted holes so that the remaining structure consisted of the host material with a periodic variation in permittivity that corresponded to a diamond-like cross-section. While this structure was shown to exhibit a complete bandgap, it proved difficult to fabricate and was not readily amenable to mass fabrication. For this reason, fabrication methods based on planar processes were pursued and developed. One such process relied on oxidation and selective etching III-V materials. With the advent of silicon-on-insulator (SOI) technology, however, a natural platform for two-dimensional PhC structures has become readily available. In this process, an SOI wafer, which consists of a layer of silicon placed on a layer of glass supported by a silicon substrate, is patterned using a high-resolution lithography system, and subsequently etched down to the glass layer. The advantage to this approach is that glass forms a natural etch stop for the etch process, so that one need only develop an anisotropic etch process, or one that insures vertical side walls. One of the reasons the SOI process is receiving a lot of attention is the availability of commercial SOI foundries within the silicon industry. Thus, methods developed using SOI promise a straightforward path to the integration of PhC devices into the existing manufacturing infrastructure. In addition, active devices

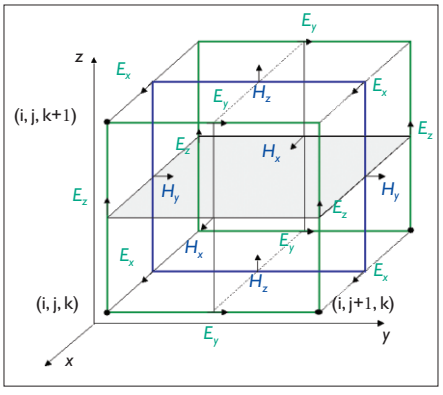


**Figure 2**. Illustration of the computational domain of the FDTD method.

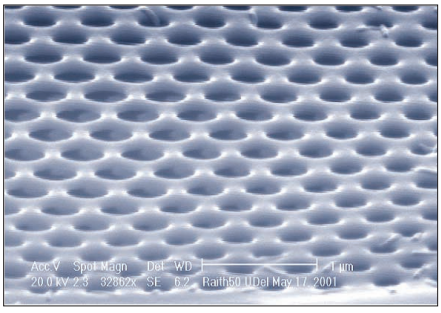


**Figure 3**. Scanning electron microscope image of a triangular photonic crystal lattice in PMMA.

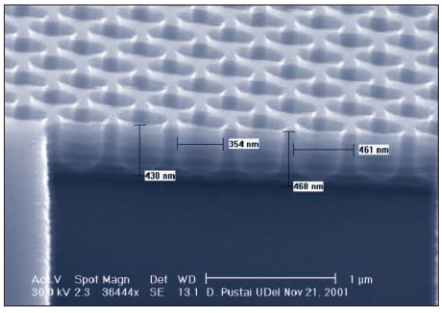


**Figure 4**. Scanning electron microscope image of a triangular photonic crystal lattice etched into a 450-nm-thick device layer SOI wafer.

such as CMOS circuits for driving and receiving optical signals can be monolithically integrated with the PhC device. As a result, now more than ever before, chip-scale photonic networks are within reach. In the remainder of this section we will discuss some of the more salient issues of the fabrication process.

Electron beam ("ebeam") lithography is typically the method of choice when it comes to generating and exposing PhC structures on SOI substrates. Alternative systems include deep UV mask aligners and steppers; in this case, however, a mask must first be made, and this is typically done using an ebeam system.

The advantage to the use of a stepper is that they are also found in standard semiconductor foundries, which eases the transition from process development to actual manufacturing. In the exposure process, variables such as PMMA (electron-sensitive material) thickness and beam proximity, among others, tend to limit the quality and resolution of the exposed pattern. For this reason, process development consists of exploring ranges of these parameters until a repeatable, high-fidelity exposure process is obtained (see Fig. 3).

Once a high-resolution lithography process has been developed, an "etch recipe," or in other words a process to transfer the exposed pattern into the underlying substrate, must be developed. This is typically done using a dry-etch technique, because of the ability it offers to transfer patterns with high aspect ratios. This is important because planar PhCs typically consist of arrays of high-fill-factor geometries whose sidewalls are very thin. In an isotropic process, these sidewalls would be etched through, thereby destroying the PhC structure. In a dry-etch process, the aim is to separate the gaseous molecules into reactive species, which are flowed over the sample under vacuum, and a radio frequency bias is applied. These reactive ions, in turn, chemically etch the surface of the sample. The ratio of flow rate of the gases (power and pressure) must be experimentally determined, because these factors dictate the selectivity of the etch process and thereby the fidelity of pattern transfer into the underlying substrate.

To achieve a dry etching process that offers a high degree of anisotropy, one can use a Bosch-like process that consists of a three-step etch cycle repeated a number of times to obtain the desired etch depth. First, a sidewall passivation polymer film is deposited using $CHF_3$ gas. This step is followed by two etch steps that use a mixture of $SF_6$ and He gases. The passivating film prevents the Si sidewalls from being isotropically etched by the $SF_6$ discharge, which contains a large concentration of atomic fluorine.

During the subsequent etch step, "the smash," or in other words the passivation polymer film, is preferentially removed from the horizontal surfaces using high energy ion bombardment in a $SF_6$ and He plasma. In the second etch step, the $SF_6$ and He plasma, which contains a large concentration of atomic fluorine, etches the silicon in the preferred downward direction, while the passivation polymer prevents sidewall etching.

The experimental variables that must be controlled to arrive at an acceptable process include RF power, etch time, smash time, gas composition, etch pressure, deposition time, gas flow rates, and chamber conditions. Once these variables have been determined, this process provides high selectivity etching, which results in vertical sidewalls, as shown in Figs. 4 and 5.

With the design tools and fabrication methods in place, the next step is to engineer PhC devices that overcome the barriers to full-scale deployment of PhC in chip-scale photonic systems. At the top of this list is the ability to efficiently couple light into and out of PhC devices. Methods for addressing this problem are discussed next.

## Coupling methods

One of the largest obstacles preventing the widespread use of planar photonic crystal devices is the difficulty of efficiently coupling light into them. The main reason lies in the enormous mode mismatch between a typical incident field and that of a PhC channel waveguide. As a result, when direct coupling is attempted, the small mode overlap results in low-efficiency coupling. Currently, among the experimental coupling methods reported in the literature, coupling losses range from ~20 to 30 dB, or in other words, typically less than one percent of the optical power ends up in the photonic crystal channel. This level of loss is unacceptable if photonic crystal devices are to be of practical use in next-generation optoelectronic systems. As a result, this area of PhC research has been especially active.

To achieve efficient coupling into a PhC device, it may be best to develop and implement a two-tier approach. In this approach, the coupling from free space, or an optical fiber, is addressed with one device, and then, once the light is in the planar dielectric slab, a second device is used to couple light into the PhC device. To this end, our group has developed a new device focused on the coupling of a slab mode to a single PhC channel defect. The

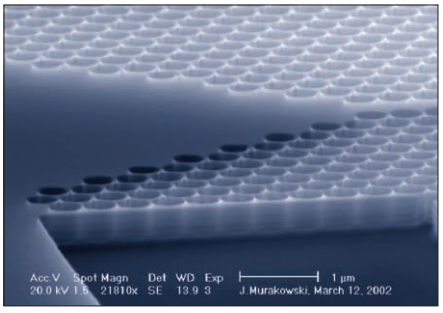


**Figure 5**. Scanning electron microscope image of an etched, high-fill-factor photonic crystal lattice that serves to illustrate the potential of a sequential etch process.

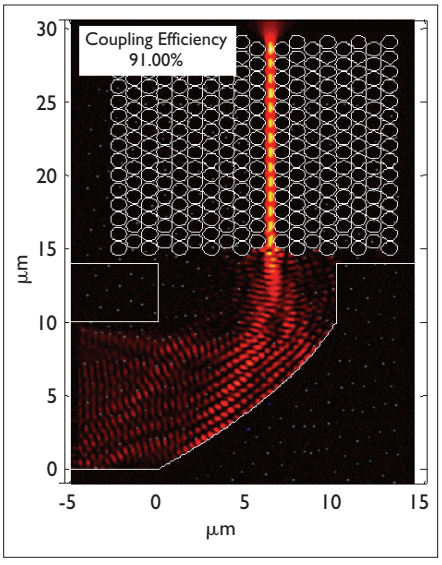


**Figure 6**. Simulation of a parabolic coupling structure for coupling from a 10-µm-wide silicon waveguide into a single-defect photonic crystal device.

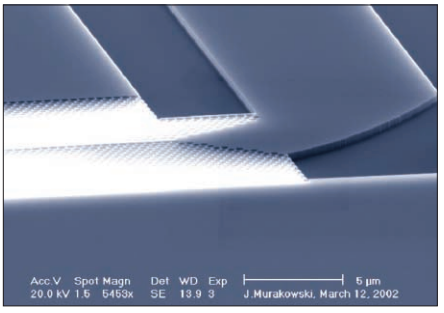


**Figure 7**. Scanning electron microscope image of a fabricated J-coupler.

device is simple, yet effective, in coupling light into photonic crystal waveguides. This result is achieved by design of a reflective structure that focuses light from a "feed" waveguide into a photonic crystal channel (see Fig. 6). We refer to this device as the J-coupler because of its resemblance to the letter J. In essence, the J-coupler is a planar version of an offset parabolic mirror, familiar from the study of large-scale geometrical optics as well as from that of microwave antennas, where a satellite dish is a good example. Computer simulations using the finite-difference time-domain method confirm the unique advantages of this approach, which offers coupling efficiencies upwards of 90%.

The device is also broadband and polarization independent, assuming the channel upon which it is focused is also polarization independent.

The J-coupler consists of a reflecting structure fabricated in a high dielectric, or "feed" waveguide that efficiently focuses the light into a single-defect photonic crystal channel (see Figs. 6 and 7). A key feature of the J-coupler is that it is a *planar* structure and, consequently, is easily fabricated using standard microelectronic techniques.

Early experimental results indicate that coupling efficiencies approaching 50% into a slab PhC single-defect channel are possible. Once this device, or a similar device, is developed and refined, additional methods that couple light from outside the wafer into the dielectric slab must be developed. To achieve this, we refer back to the techniques developed during the late 1970s and the 1980s for coupling into low dielectric constant waveguides. During this era, several very efficient coupling methods were developed based on gratings, tapers, and prisms.

Clearly, the problem of coupling into silicon slabs will be more difficult, however, the same principles can be applied and modified for applications to PhC devices. Once the problem of efficient coupling is solved, the next pressing technological challenge is integration, discussed next.

## Integration methods

To paraphrase a saying from the great Vince Lombardi, "Integration is not everything, it is the only thing." By this I mean that in the stages of PhC development described above, one must focus not only on improved process and device performance but also on their efficient, reliable, and economic integration into the current manufacturing infrastructure.

While great progress is being made thanks to increased interaction with semiconductor foundries, additional factors must be addressed: for instance, hybrid integration of external sources and, possibly, detectors with PhC devices and systems. The good news here is that such hybrid integration techniques, including flip-chip bonding, are becoming increasingly more common in the microelectronics industry. For this reason, a high degree of leverage can be achieved between electronic integration processes and those needed for optoelectronic integration.

While the integration processes involved in some aspects of these technologies may be identical, in others they may be very different. For instance, in the development of packaging of electronics, the aim is to lower cost, increase packaging density, and improve performance while maintaining or even improving the reliability of the circuits. To a large extent, these goals are common to both technologies. However, in the case of optoelectronic integration, certain aspects of the process become more important than in the electronic case.

One example is alignment of an output optical beam to the host flip-chip substrate. In the electronic case, one is only interested in making electrical contact; in the optoelectronic case, on the other hand, it is important to make not only electrical contact but also to achieve optical alignment. Typically this can be done by creating self-aligning structures in addition to electronic contacts.

The field of PhCs is not yet at the integration stage but it soon will be. At that point the issues discussed will become paramount to enabling the widespread use of the technology.

In closing, in this article we have presented an engineering perspective of the field of photonic crystals. To this end, we have discussed some of the key application areas. We have also discussed several aspects of the technology and tried to present not only a snapshot of the state of the art, but also a glimpse of the past. In addition to the issues raised here, there are many more that were not addressed.

Despite all of the uncertainty in the field, the potential is tremendous and once the technical challenges are resolved, the only limitation will be our imagination.

**Dennis Prather is an associate professor at the University of Delaware in the Department of Electrical and Computer Engineering, where he has established the Laboratory for Integrated Photonic Systems. His e-mail address is dprather@ee.udel.edu.**